3AXT8500C5-4096K
240-Pin PC2-8500 DIMM
2x2GB 256M x 64-bit CL5

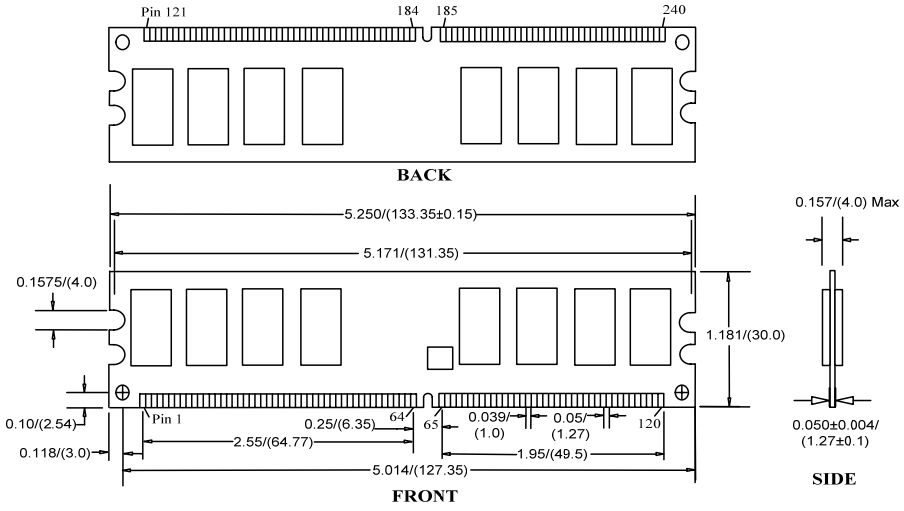
DESCRIPTION:

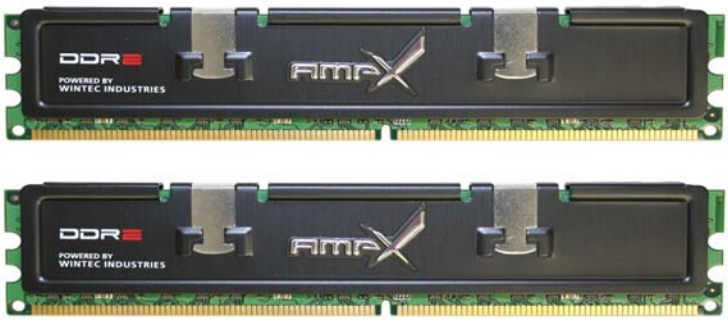
This data sheet describes Wintec's 2x2GB DDR2-1066 SDRAM (Synchronous DRAM) DIMMs as a kit. It contains sixteen 128Mx8-bit 800MHz DDR2 60-ball FBGA components. Each module has been tested to run at DDR2 1066MHz at latency timing of 5-5-5-15 at 2.2V. The SPD is programmed to JEDEC standard DDR2 800MHz and latency timing of 5-5-5-15 at 1.8V. It uses gold plated contact fingers and requires power supply of 1.8V. The electrical and mechanical specifications are shown below:

PERFORMANCE:

➢ Clock Cycle Time (tCK) @ CL5	2.5ns (min.) / 8ns (max.)
➢ Row Cycle Time (tRC)	57.5ns (min.)
➢ Refresh to Refresh command interval (tRFC)	127.5ns
➢ Row Active Time (tRAS)	45ns
➢ Active to Read/Write delay (tRCD)	12.5ns
➢ Precharge command period (tRP)	12.5ns
➢ Operating Temperature at Case	0°C to +85°C

LAYOUT:





* Please check your manual or the motherboard manufacturer for additional chipset and over-clocking information. Performance varies across all models and motherboards, as not all systems can achieve the full 1066 MHz of PC2-8500 at CAS Latency 5-5-5-15